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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,168	10/30/2001	Makoto Ono	16869P-037300US	8661

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,168	ONO ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,24,27,28,31 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,24,27,28,31 and 36-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 21 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Berezin (US Patent 5,777,901)..

3. As for claim 21, Berezin disclosed the invention substantially as claimed, including an inspection system comprising

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected [col. 1, lines 40-55];

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus [col. 1, lines 40-55; fig. 1; col. 4, lines 58-67];

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus, said analysis unit including [col. 4, lines 58-67]:

a storage device for storing therein inspection data produced by said inspection apparatus and position information of regions of a circuit pattern to be formed on said object [col. 6, lines 33-55, the defect records are stored by the scan tool];

a calculation device for identifying particle and pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities for said

particles and said pattern defects positioned in said regions based on their sizes [col. 3, lines 23-45; failure probabilities are calculated based on at least size]; and

a selection device for selecting particles or pattern defects for calculated failure probabilities whose calculated failure probabilities are greater than or equal to a predetermined threshold [col. 3, lines 22-45, defect types are preselected for the failure probability calculation; col. 5, lines 3-11,].

4. As for claim 36, Berezin disclosed the invention substantially as claimed, including a method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer, said circuit patterns constituting a plurality of semiconductor chips [col. 1];

an inspection step for detecting positions and sizes of particles or pattern defects on an said wafer [col. 1, lines 40-55];

identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns that constitute one of said semiconductor chips [col. 1, lines 40-55; col. 2, lines 64-67; col. 3, lines 1-3, 10-12, 20-26];

a calculation step for calculating failure probabilities based on sizes of said pattern defects in said region [col. 3, lines 23-45; failure probabilities are calculated based on at least size];

an extraction step for extracting positions of said particles or said pattern defects with calculated failure probabilities greater than or equal to a predetermined threshold [col. 3, lines 54-57, the wafer map includes position information of the particles or pattern defects; col. 5, lines 5-11]; and

producing images of said particles or said pattern defects extracted at said extraction step [col. 3, lines 54-57; col. 1, lines 63-65; col. 8, lines 43-48].

Claim Rejections - 35 USC § 103

5. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berezin (US Patent 5,777,901) in view of Atchison (US Patent 6,324,481).

6. As for claim 27, Berezin disclosed the invention substantially as claimed, including the system and method for inspecting defect positions and sizes of defects within a semiconductor wafer and die as cited in the rejection of claims 21 and 36 above.

Berezin did not specifically disclose a simulation device for generating virtual defects at random positions with respect to circuit graphics obtainable from mask layout data forming said circuit pattern, and computing said failure probabilities from connection relationships of said circuit graphics and said defects.

Atchison disclosed a simulation device for generating virtual defects at random positions with respect to circuit graphics obtainable from mask layout data forming said circuit pattern, and computing said failure probabilities from connection relationships of said circuit graphics and said defects [col. 5, lines 1-15, and 52-67; and col. 6, lines 1-7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Berezin and Atchison because Atchison's simulation would have improved Berezin's system by allowing for the calculation of critical area for Berezin's layers and therefore would have allowed for the accurate prediction of layer yield probability [see Atchison, col. 5, lines 19-37].

7. Claims 24, 28, 31, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berezin (US Patent 5,777,901) in view of Hashimoto (US Patent 6,334,209).

8. Claims 24, 28, 31, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berezin (US Patent 5,777,901) in view of Hashimoto (US Patent 6,334,209).

9. As for claims 24, 28, 31, and 37-38, Berezin disclosed the invention substantially as claimed, including the method and apparatus for inspecting semiconductor devices as cited in the rejections of claims 21 and 36 above

Berezin did not specifically disclose circuit blocks are formed as a (system) LSI chip and include memory and logic portions, said position information of said regions is generated from mask layout data forming an LSI chip.

Hashimoto disclosed a system LSI with logic and memory portions and mask layout data [col. 3, lines 50-54; and col. 9, lines 50-60].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Berezin and Hashimoto because Berezin disclosed the inspection system and method including semiconductor chips as cited in the rejection of claims 21 and 36 above that comprise integrated circuits such as LSI's, and Hashimoto disclosed system LSI's including logic and memory portions. The inspection of circuit blocks within system LSI's and the position information of said regions which is generated from mask layout data of circuit blocks would have allowed Berezin's inspection system to evaluate defect conditions of well known circuits such as the LSI for the manufacturing of good circuits with as little defect as possible.

10. Applicant's arguments with respect to claims 21, 24, 27-28, 31, and 36-38 have been considered but are moot in view of the new ground(s) of rejection.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
November 24, 2003